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Compensation of Unbalanced Three Phase Currents in a Transmission line using Distributed Power Flow Controller

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ABSTRACT

Distributed Power Flow Controller is a new device within the family of FACTS. The DPFC has the same control capability as the UPFC, but with much lower cost and higher reliability. This paper addresses one of the applications of the DPFC namely compensation of unbalanced currents in transmission systems. Since the series converters of the DPFC are single phase, the DPFC can compensate both active and reactive, zero and negative sequence unbalanced currents. To compensate the unbalance, two additional current controllers are supplemented to control the zero and negative sequence current respectively.

Keywords **- DPFC, Unbalanced currents, Zero sequence**

I. INTRODUCTION

Power Quality is becoming an important issue for both electric utilities and end users [1]. Unbalanced voltages and
currents in a network are one of the concerns under the power quality issue. The unbalance is mainly produced by the great number of single-phase loads which are unevenly distributed over the phases [2]. The unbalance voltages can cause extra losses in components of the network, such as generators, motors and transformers, while unbalanced currents cause extra losses in components like transmission lines and transformers [3]. Active filters and power factor corrector can be applied to compensate the unbalance at the load side, however their contributions to transmission systems is not large because they are focused on single load [4], [5]. FACTS devices can be employed to compensate the unbalanced currents and voltages in transmission systems. Unfortunately, it is found that the capability of most of FACTS devices to compensating unbalance is limited. Series and shunt FACTS device can only provide compensation of unbalanced reactive currents [6], and the most powerful device – the UPFC [7] cannot compensate zero-sequence unbalance current, because of the converter topology [8]. This paper will show that the so-called DPFC can compensate both active and reactive, zero and negative sequence unbalanced currents.

The Distributed Power Flow Controller (DPFC) recently presented in [9], is a powerful device within the family of FACTS devices, which provides much lower cost and higher
reliability than conventional FACTS devices. It is derived from the UPFC and has the same capability of simultaneously adjusting all the parameters of the power system: line impedance, transmission angle, and bus voltage

magnitude [7]. Within the DPFC, the common dc link between the shunt. and series converters is eliminated,
which provides flexibility for independent placement of series and shunt converter. The DPFC uses the transmission
line to exchange active power between converters at the 3rd harmonic frequency [9]. Instead of one large three-phase converter, the DPFC employs multiple single-phase converters (D-FACTS concept [10]) as the series compensator. This concept not only reduces the rating of the components but also provides a high reliability because of the redundancy. The scheme of the DPFC in a simple two-bus system is illustrated in Fig.1.

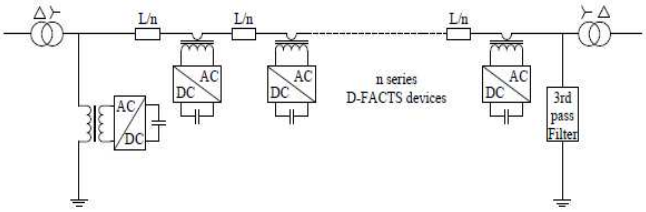

Fig. 1. Distributed power flow controller

As the series converters of the DPFC are single-phase, it gives the DPFC the opportunity to control current in each phase independently, which implies that both negative and zero sequence unbalanced current can be compensated. The objective of this paper is to investigate the capability of the DPFC to balance the network. Additional controllers are supplemented to the existing DPFC controller. Their control
principle is to monitor the negative and zero sequences current through the transmission line and to force them to be zero.

II. PRINCIPLE OF THE DPFC

Multiple individual converters cooperate together and compose the DPFC. The converters connected in series to the transmission lines are the series converters. They can inject a controllable voltage at the fundamental frequency; consequently they control the power flow through the line. The converter connected between the line and ground is the shunt converter. The function of the shunt converter is to compensate reactive power to the grid, and to supply the active power required by the series converter. In a normal UPFC, there is active power exchange through the DC link that connects the series converter with the shunt converter. Since there is no common dc link between the shunt and series converters in the DPFC, the active power is exchanged by harmonics and through the ac network. The principle is based on the definition of active power, which is the mean value of the product of voltage and current, where the voltage and current comprise fundamental and harmonics. Since the integrals of all the cross-product of terms with different frequencies are zero, the time average active power can be expressed by:

$$P = \sum_{n=1}^{\infty} VnIn\cos\phi n \quad (1)$$

where n is the order of the harmonic frequency and φn the angle between the current and voltage of the nth harmonic. Equation 1 describes that active powers at different frequencies are isolated from each other and that voltage or current in one frequency has no influence on other frequency components. The 3rd harmonic is chosen here to exchange the active power, because it can easily be filtered by Y-Δ transformers.

III. DPFC CONTROL SCHEME FOR UNBALANCE COMPENSATION

The DPFC is a complex system, which contains multiple control loops for different purposes. This section introduces the DPFC control concept firstly, and discusses the supplementary controller for unbalance compensation in detail.

A. Introduction of the DPFC primary control scheme

The shunt converter injects a constant 3rd harmonic current into the transmission line, which is intended to supply active power for the series converters. The shunt converter extracts some active power from the grid at the fundamental frequency to maintain its dc voltage. The dc voltage is controlled by the *d* component of the fundamental current, and the *q* component is utilized for reactive power compensation. The series converters generate a 360◦ rotatable voltage at fundamental frequency, and use the voltage at the 3rd frequency to absorb active power to maintain their dc voltages. The block diagram of the DPFC and its control is shown in Fig.2.

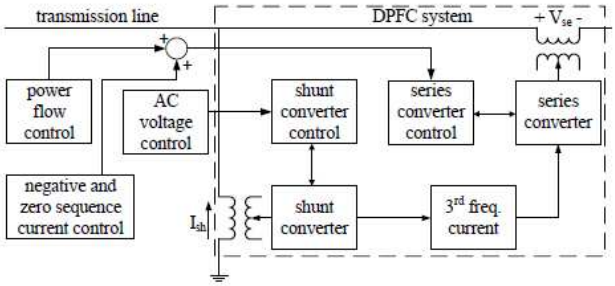

Fig. 2. Block diagram of the control of a DPFC

The series converter control block generates PWM signal according to the reference and maintains the capacitor dc voltage. The power flow control block is placed at the shunt converter side, and generates the control signals for the series converters according to the power flow reference at the fundamental

frequency. The control signals are transmitted to series converters remotely and independent.

B. DPFC control scheme for unbalance compensation

The principle of DPFC unbalance compensation is to measure the zero and negative sequence current through the line and to force them to be zero by an opposing voltage. Two current controllers are supplemented to the existing controllers and responsible for the zero and negative sequence current respectively, as shown in Fig.2. The current reference for the zero and negative sequence is zero constantly. During unbalanced situation, the two current controllers generate compensating zero and negative sequence voltage signals for the series converters; these are transmitted together with the positive voltage signals to the series converters. Consequently, the unbalanced currents through the line are compensated. The block diagram of the control scheme for unbalance compensation is shown in Fig.3.

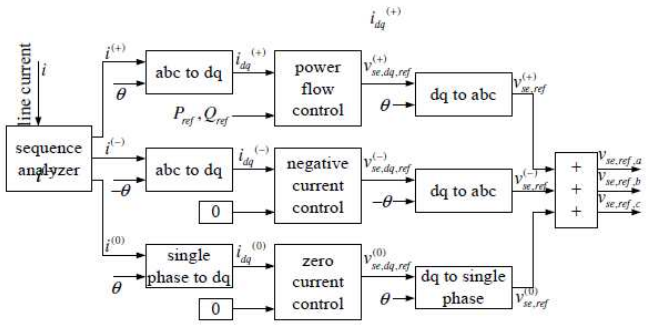

Fig.3. Control scheme for unbalance compensation

The sequence analyzer distinguishes the sequence components of the line current. By using Park-transformation, the AC current are transformed to dc quantities. The three controllers generate voltage signal for each sequence according to their references, and the signals are converted back to AC quantities which is used to control the series converters.

C. Zero and negative sequence current controller design

A popular method for current control - synchronous PI control - is employed for the zero and negative sequence controller, because of the simplicity of the implementation [11]. The idea is to transform currents and voltages into a rotating reference frame, where the controlled currents are constant in 'steady-state', use ordinary PI controllers on the transformed values, and transform the controller outputs back to the fixed reference frame.

The structures of the zero and negative sequence network with the DPFC are similar. By replacing the DPFC series converter by ideal voltage sources, the simplified zero and negative sequence network with the DPFC can be represented as Fig.4.

Here $v_0^{u,-}$ is the unbalanced zero and negative sequence voltage in the network, $i_0^{u,-}$ is the corresponding unbalanced current within the line, $R_l^{0,-}$ and $L_l^{0,-}$ are zero and negative sequence network resistance and inductance respectively, and $v_{se}^{0,-}$ is the unbalance compensation voltage generated by the series converter. With the dq-transformation, the current and voltage have the relationship:

$$v_{se,d}^{0,-} = R_l^{0,-} i_{u,d}^{0,-} + L_l^{0,-} \frac{di_{u,d}^{0,-}}{dt} - \omega L_l^{0,-} i_{u,d}^{0,-} - v_{u,d}^{0,-}$$

$$v_{se,q}^{0,-} = R_l^{0,-} i_{u,q}^{0,-} + L_l^{0,-} \frac{di_{u,q}^{0,-}}{dt} + \omega L_l^{0,-} i_{u,d}^{0,-} - v_{u,q}^{0,-}$$

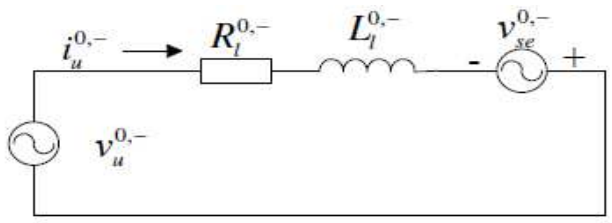

Fig. 4. Simplified zero and negative sequence network with the DPFC

The cross coupling and the unbalanced voltage can be as disturbances, and the transfer function form voltage $v_{se}^{0,-}$ to current $i_l^{0,-}$ for both d and q components can be found as:

$$G(s) = \frac{1}{Rl + sLl} \qquad (2)$$

The current control parameter is calculated by internal model control (IMC) method [12], [13]. As

the disturbance (unbalanced voltage) is unpredictable, additional inner feedback loops are added to active damp the disturbance for each control loop. Accordingly, the control scheme of the unbalanced current compensation is illustrated in Fig.5: where $F(s)$ is the

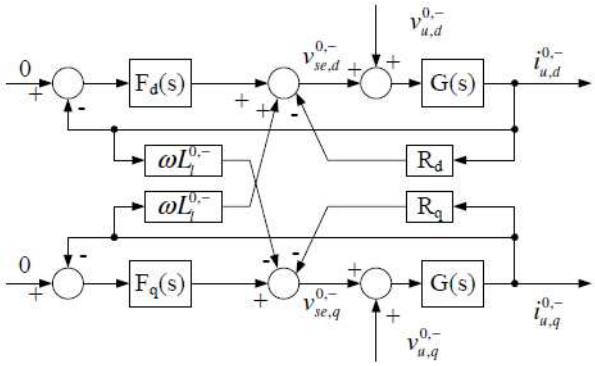

Fig. 5. Control scheme of the unbalanced current compensation

controller function that can be calculated by the IMC method as:

$$F_d^{0,-}(s) = \alpha_d^{0,-} L_l^{0,-} + \alpha_d^{0,-}(R_l^{0,-} + R_d^{0,-})/s$$
$$F_q^{0,-}(s) = \alpha_q^{0,-} L_l^{0,-} + \alpha_q^{0,-}(R_l^{0,-} + R_q^{0,-})/s$$

where α_d and α_q are the bandwidth for d and q components control respectively. The parameter α is a design parameter that determines the desired bandwidth of the closed-loop system here. The relationship between the bandwidth and he rise time trise (from 10% to 90% of the final value) is [13]:

$$\alpha = \frac{\ln 9}{Trise} \qquad (3)$$

The active damping is properly designed if it has the same time constant as the control loop, therefore the active conductance for each control loop can be found as:

$$R_d^{0,-} = \alpha_d^{0,-} L_l^{0,-} - R_l^{0,-}$$
$$R_q^{0,-} = \alpha_q^{0,-} L_l^{0,-} - R_l^{0,-}$$

IV. SEQUENCE NETWORK ANALYSIS WITH THE DPFC

In order to compensate the unbalance, the series converters of each phase generate different voltages, and require different active powers consequently. As the DPFC uses 3rd harmonic current to exchange active power between the shunt and series converters, this unbalance compensation will have an influence to the 3rd harmonic current. This section studies the behavior of a simple network with the DPFC under the unbalance situation, by using the method of symmetrical components introduced by C.L. Fortescue [14].

Fig.6 shows the circuit configuration of the DPFC connected to a simple power system which consists of two power grids with symmetical voltage v_s ,v_r and a tie-line. The shunt converter of the DPFC is a back-to-back converter, which absorbs active power from the low voltage side and injects 3rd harmonic current through the neutral point of the Y-Δ transformer. The multiple series converters are represented by three single-phase converters for each phase. An unbalanced voltage v_u is added at the grid s.

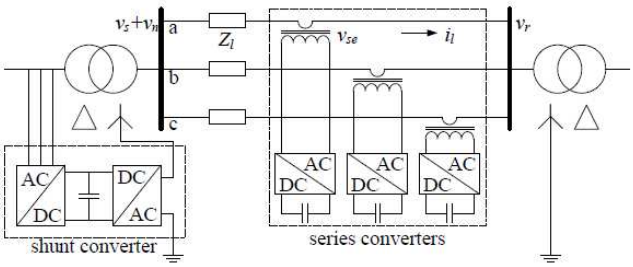

Fig. 6. Circuit configuration of the DPFC connected to a simple power
system

To simplify the analysis, it is assumed that v_u contains the negative and zero sequence component, and $v_{+u} = 0$. Without the unbalance compensation, the current through the line can be represented in sequence components:

$$\begin{bmatrix} i_l^+ \\ i_l^- \\ i_l^0 \end{bmatrix} = \begin{bmatrix} 1/Z_l^+ & 0 & 0 \\ 0 & 1/Z_l^- & 0 \\ 0 & 0 & 1/Z_l^0 \end{bmatrix} \begin{bmatrix} v_s - v_r \\ v_u^- \\ v_u^0 \end{bmatrix}$$

To compensate the unbalance, the DPFC series converter will generate a voltage which is opposite to v_u:

$$v_{se} = v_{se}^{+} - v_u \qquad (4)$$

where v_{se} is the voltage generated by the series conveters at fundamental frequency; and its positve sequence component is for power flow control. The active power at the fundamental frequency required by each series converter is written in (9).

As shown in (9), when the DPFC completely compensates the unbalance, the active power requirement for the series converters can also be analyzed according to the sequences.

The zero sequence compensation at the fundamental frequency leads to negative power requirement, and negative sequence leads to positive sequence requirement. The active power supplied by the 3rd harmonic frequency current can be written as (10), where V_u^{o} , V_u^{-} , V_{se}^{+} and I_l^{-} are the magnitude of v_u^{0}, v_u^{-} , v_{se}^{-} and i_l^{+} respectively. The angle θ is the angle between v_{se+} and i_l^{+} . The 3rd harmonic current is zero sequence components and blocked by the Y-Δ transformers. However, during the unbalance compensation, unsymmetrical active power is required by the series converters, which causes positive and negative sequence current at 3rd harmonic. Since the positive and negative 3rd harmonic current cannot be blocked by the transformers, it is important to find out whether there magnitudes are acceptable for the network from the viewpoint of power quality.

The equivalent network of the DPFC at the 3rd harmonic can be represented as Fig.7. To reduce the magnitude of the3rd harmonic current through the line, the series converter will not generate any reactive power at the 3rd frequency. Therefore the series converters can be considered as resistances [R_a R_b R_c] at the 3rd frequency, the power consumed by the resistors are [$P_{se,3}$]. The shunt converter is controlled as a current source, which injects a constant current i_3 to the neutral point. Consequently, the 3rd harmonic frequency circuit can be expressed by the following equations:

$$\begin{cases} i_{a,3} + i_{b,3} + i_{c.3} = i_3 \\ Z_{l,3} \cdot i_{a,3} + \frac{P_{sc,a,3}}{i_{a,3}^{*}} = V \\ Z_{l,3} \cdot i_{b,3} + \frac{P_{sc,b,3}}{i_{b,3}^{*}} = V \\ Z_{l,3} \cdot i_{c,3} + \frac{P_{sc,c,3}}{i_{c,3}^{*}} = V \end{cases}$$

As equation (11) is not linear, it is difficult to achieve analytical solutions for the 3rd harmonic current[$i_{a,3}$ $i_{b,3}$ $i_{c,3}$]. However, by applying a some typical DPFC parameters and solving the equations numerically, it is found that the nonzero sequence 3rd current [$i_{a,3}$ $i_{b,3}$ $i_{c,3}$]+- is less than 10% of nominal line current, typically around 4%.

V. SIMULATION RESULTS

The simulation of application of the DPFC to compensate unbalance has been done in Matlab, simulink. The system shown in Fig.6 is used as a test example. The magnitudes of the voltages at grid is 1pu, and v_s leads v_r 1.5°. The transmission line is represented by a 0.06pu inductor, and the resistance is neglected. Accordingly, the power flow of the system without compensation is around P=1pu, and Q=- 0.06pu from *s* to *r* grid. In the simulation, the power flow is

limited by the DPFC to P=0.4pu and Q=0pu. And the DPFC uses constant 0.4pu 3rd harmonic current to exchange active
powers between the shunt and series converters. To simulate the unbalanced condition, an unbalanced voltage v_u is added at grid s at the moment t=1s, and both the zero and negative components of v_u contain 1% unbalances. The unbalance compensation controllers of the DPFC are switched off before t=1.5s. Fig.8 illustrates the current through the line at the fundamental frequency in both real-time and magnitude formats.

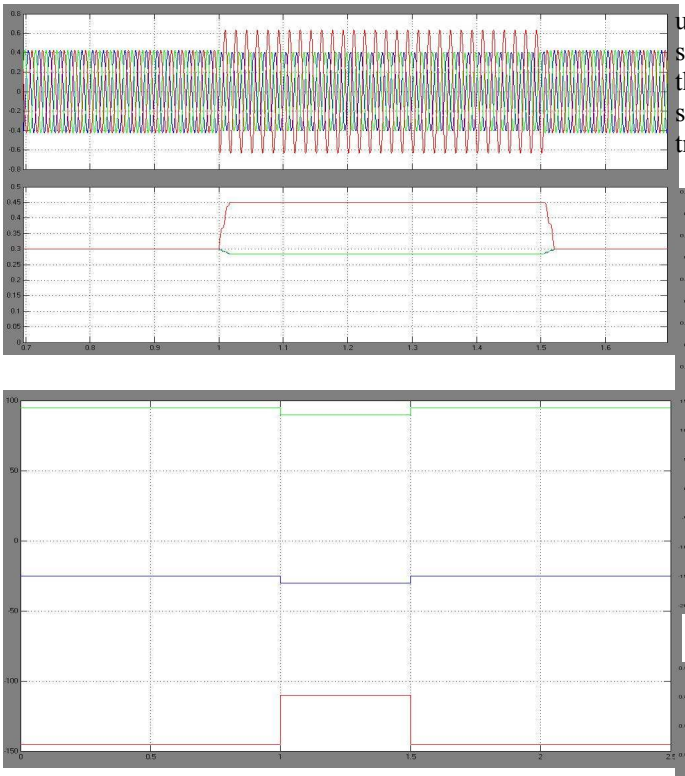

Fig. 8. The current through the line at the fundamental frequency

As shown, during the unbalance condition, both the magnitude and angle of the line current considerable changed without the compensation; the current magnitude in phase *a* increased almost 75%. With the compensation, the unbalanced current is totally compensated by the series converters. The voltages injected by the series converter are shown in Fig.9.

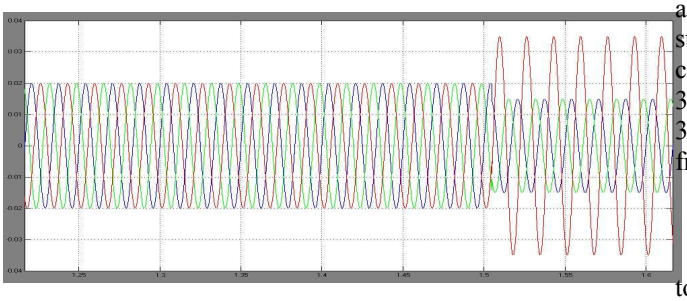

Fig. 9. The voltages injected by the series converter

To compensate the unbalance, the series converters generate unsymmetrical voltages, as shown in Fig. 9. Consequently, the 3rd harmonic currents which are used to supply the active power will contain non-zero sequence components. The magnitude and angle of the 3rd current is shown in Fig.10, and the nonzero sequence 3rd currents, which cannot be blocked by transformers, are illustrated in Fig.11.

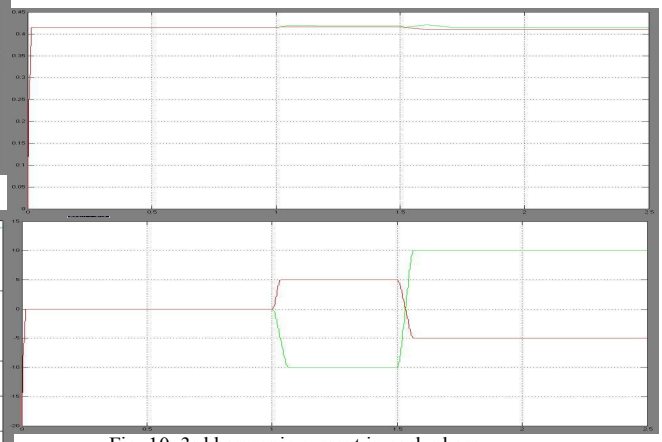

Fig. 10. 3rd harmonic current in each phase

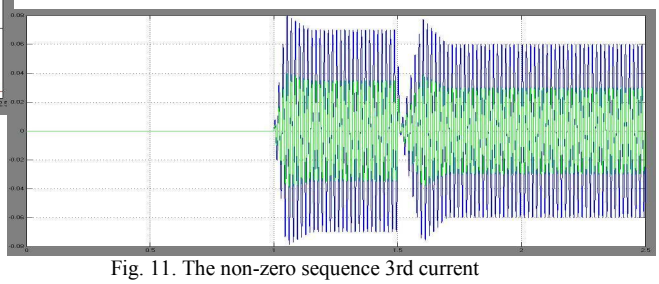

Fig. 11. The non-zero sequence 3rd current

As shown in Fig.11, around 0.03pu non-zero sequence 3rd harmonic is generated by the DPFC system. The appearance of this current is not only caused by the unbalance compensation control, but also the unbalance at the fundamental frequency. The supplementary controllers for the unbalance compensation do not increase the non-zero sequence 3rd current. The magnitude of the non-zero sequence 3rd is much smaller than the current at fundamental frequency, less than 4%.

VI. CONCLUSIONS

This paper investigates the capability of the DPFC to balance a network. It is found that the DPFC can compensate both negative and zero sequence components, consequently the DPFC is more powerful than other FACTS device for compensation of unbalanced currents. Additional controllers are supplemented to existing DPFC controller, and their principle is to monitor the negative and zero

sequences of the current through the transmission line, and to force them to be zero by applying an opposing voltage. As a side effect, the DPFC generates non-zero sequence 3rd current during the unbalance situation, which can not be blocked by the Y-Δ transformer. However the magnitude of the non-zero sequence 3rd current is much smaller than the nominal current at the fundamental frequency, less than 4% typically.

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